REMARKS

The Applicant thanks the Examiner for his careful and thoughtful examination of the present application. By way of summary, Claims 1-20 were pending in this application. In this response, the Applicant has amended Claims 1, 17 and 18. Accordingly, Claims 1-20 remain pending for consideration.

OBJECTION TO CLAIM 18

The Office action objected to Claim 18 for minor informalities. In particular, the Office action pointed out that Claim 18 recited "b) because." Applicant appreciates that the Examiner brought this spelling error to Applicant's attention. In response, the Applicant has amended Claim 18 to recite "b) cause." Accordingly, Applicant respectfully requests withdrawal of the objection to Claim 18.

REJECTION OF CLAIMS 1-3, 10-12, 14 AND 17 UNDER 35 U.S.C. § 102(e)

The Office action rejected Claims 1-3, 10-12, 14 and 17 under § 102 as being anticipated by U.S. patent application publication no. 2004/0148470, by Schulz (Schulz). Applicant respectfully traverses this rejection because Schulz fails to identically teach every element of the rejected claims. *See* M.P.E.P. § 2131 (stating that in order to anticipate a claim, a prior art reference must identically teach every element of the claim).

For example, amended Claim 1 now recites: "a cache demand circuit adapted to: receive a memory address and a memory access signal, and cause the micro-controller cache system to fetch data stored in the received memory address from the remote memory via the buffer manager based on the received memory address and memory access signal prior to a micro-controller request for the data stored in the received memory address." Schulz neither teaches nor discloses this limitation.

With respect to this limitation of Claim 1 in unamended form, the Examiner had cited page 4, paragraph [0040] and page 6, paragraph [0058] of Schulz as teaching this structure. However, these passages of Schulz merely disclose the well-known caching methodology of using a first address of a first memory request to pre-fetch information

at one or more pre-fetch addresses calculated from the first memory request address, which pre-fetch information may later be requested by the processor, as discussed in the background of Applicant's specification (p. 1, ll. 22-24). In particular, Schulz teaches that "[w]hen pre-fetching is enabled, the address of the current memory request may be used as a base address n. Depending on which bits are selected within configuration storage 151, one or more pre-fetch addresses are calculated by pre-fetch address calculation logic." Paragraph [0052] (emphasis added). Schulz then teaches that the "pre-fetch unit 150 may issue a pre-fetch request for each matching pre-fetch address to control unit 120" (paragraph [0058]), which pre-fetch requests are based on the calculated pre-fetch addresses. Schulz does not teach or suggest a cache demand circuit adapted to receive a memory address and cause the micro-controller cache system to fetch data stored in the received memory address (rather than in a calculated memory address based on the received memory address) prior to a micro-controller request for the data stored in the received memory address.

For at least these reasons, the rejection of Claim 1 as anticipated by Schulz is improper.

Amended Claim 17 similarly recites: "a cache demand circuit adapted to: receive a memory address and a memory access signal from the micro-controller, and cause the micro-controller cache system to fetch data stored in the received memory address from the remote memory via the buffer manager based on the received memory address and memory access signal prior to a micro-controller request for the data stored in the received memory address." Schulz neither teaches nor discloses this limitation.

For reasons similar to those discussed above with respect to Claim 1, Applicant submits that Schulz neither teaches nor discloses such a cache demand circuit. For at least these reasons, the rejection of Claim 17 as anticipated by Schulz is improper.

Claims 2-3, 10-12 and 14, which depend from Claim 1, are believed to be patentable for at least the same reasons articulated above, and because of the additional features recited therein.

REJECTION OF CLAIMS 4-9, 13, 15-16 AND 18-20 UNDER 35 U.S.C. § 103(a)

The Office action rejected Claims 4-9, 13, 15-16 and 18-20 under 35 U.S.C. § 103 as being unpatentable over Schulz in view of U.S. patent no. 6,789,132, issued to Hoskins (Hoskins).

REFERENCES FAIL TO TEACH ALL OF THE CLAIMED ELEMENTS

The Applicant respectfully traverses this rejection because Schulz, alone or in combination with Hoskins, fails to teach or suggest all of the elements of the rejected claims. *See* M.P.E.P. § 2143 (stating that in order to establish a *prima facie* case of obviousness for a claim, the prior art references must teach or suggest all the claim limitations).

As discussed above, amended independent Claim 1 recites limitations that are plainly not taught or disclosed in Schulz. These limitations are also not taught or suggested by Hoskins.

Amended Claim 18 recites "a cache demand circuit adapted to: receive a predetermined memory address from the micro-controller and the transmitted interrupt signal from the interrupt circuit, and cause the micro-controller cache system to fetch data stored in the predetermined memory address from the remote memory via the buffer manager prior to a micro-controller request for the data stored in the predetermined memory address." Schulz, alone or in combination with Hoskins, neither teaches nor suggests this limitation.

For reasons similar to those discussed above with respect to Claims 1 and 17, Applicant submits that Schulz, alone or in combination with Hoskins, neither teaches nor suggests such a cache demand circuit. In particular, Schulz (alone or in combination with Hoskins) does not teach or suggest a cache demand circuit adapted to receive a predetermined memory address and cause the micro-controller cache system to fetch data stored in the predetermined memory address (rather than in a calculated memory address based on the predetermined memory address) prior to a micro-controller request for the data stored in the predetermined memory address. For at least these reasons, the rejection of Claim 18 as obvious over Schulz and Hoskins is improper.

Therefore, Claims 4-9, 13, 15-16 and 19-20, which depend from Claims 1 and 18 respectively, are believed to be patentable for at least the same reasons articulated above, and because of the additional features recited therein.

CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that the pending claims are now in condition for allowance and requests reconsideration of the rejections. If it is believed that a telephone conversation would expedite the prosecution of the present application, or clarify matters with regard to its allowance, the Examiner is invited to contact the undersigned attorney at the number listed below.

The Commissioner is hereby authorized to charge payment of any required fees associated with this Communication or credit any overpayment to Deposit Account No. 23-1209.

Respectfully submitted,

Date: January 20, 2006

By: _____
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